REMARKS

Claims 1-18 remain in this application. Claims 1 and 2 are the independent Claims. Claims 1 and 2 have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Statement of Substance of the Interview

Pursuant to the Office Communication dated June 7, 2007, a statement of the substance of the telephone interview conducted on June 1, 2007 is included herein. On June 1, 2007 Registered Patent Agent Aniket Patel conducted a telephone interview with Examiner Vincent Lay. Differences between Dowling and the present application were discussed. Examiner Lai suggested that a response to the Office Action, dated February 2, 2007, be filed consistent with the differences identified in the interview and stated he would respond in due course.

Art-Based Rejections

Claims 1-14 were rejected under 35 U.S.C. § 102(b) over U.S. Patent 6,157,988 (Dowling). Applicant respectfully traverses the rejection and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Dowling Reference

Dowling is directed to providing a pipeline architecture with a branch caching structure that reduces or eliminates pipeline stalls regardless of whether the fall-through or the target instruction is to be executed. The present architecture is

hardware efficient and involves simple parallel operations that can be performed in a short clock cycle. (*See, Dowling, col. 4, lines 15-19*)

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device using pipeline control.

As defined by amended independent Claim 1, a data processing device using pipeline control includes an instruction queue in which a plurality of instruction codes are fetched, a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue, and a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue. A branch information setting circuit which decodes a branch setting instruction, the branch setting instruction explicitly or implicitly specifies a branch address and a branch target address. A branch to the branch target address occurs when the fetch address is the branch address after a x-th instruction from the branch setting instruction. The branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded. The fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

The applied Dowling does not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, a branch information setting

circuit that specifies "a branch information setting circuit which decodes a branch setting instruction, wherein the branch setting instruction explicitly or implicitly specifies a branch address and a branch target address, wherein a branch to the branch target address occurs when the fetch address is the branch address after a x-th instruction from the branch setting instruction, the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded,

wherein the fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result," as required by amended independent Claim 1.

According to the Office Action, Dowling at col. 10, lines 13-15 and 55-58 discloses a branch information setting circuit which decodes a branch setting instruction and that when the fetch address is the branch address after x-th instruction from the branch setting instruction as defined by Claim 1 (*See, Office Action p. 4, lines 7-9 and lines 11-13*). However, Applicant respectfully submits that Dowling teaches a branch address which may mean either a branch instruction address or a branch target address (*See, Dowling, col. 9, lines 60-64; col. col. 10, lines 10-26*).

In contrast amended independent Claim 1 clarifies that, a branch address is an address in which a branch to a branch address target occurs as discussed at p. 15, lines 9 – 13 of the specification. One advantage of the present invention is that, because the branch setting instruction includes not only the branch target address

information but also the branch address information, so that a user may control the timing at which a branch occurs, thereby allowing improvement in programming freedom.

Applicant respectfully submits a branch instruction address does not teach or suggest that a branch address is an address in which a branch to a branch address target occurs. The technical term "branch address", as defined by Dowling, has a different meaning, from the term as defined by amended independent Claim 1 and as such Dowling fails to teach or suggest the branch address of the present invention.

Accordingly, Dowling fails to disclose, teach or suggest "a branch information setting circuit which decodes a branch setting instruction, wherein the branch setting instruction explicitly or implicitly specifies a branch address and a branch target address, wherein a branch to the branch target address occurs when the fetch address is the branch address after a x-th instruction from the branch setting instruction, the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded," as required by amended independent Claim 1.

Further still, according to the Office Action, Dowling at col. 13, lines 29-34, discloses that branching information is stored in registers and that this reads on "the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded," as required by amended independent Claim 1 *(See, Office Action p. 4 lines 13-17)*.

However, Dowling at column 13, lines 29 to 34 discloses storing a branch condition, with the cited portion remaining silent regarding storing a branch

address in the branch address storage register and storing a branch target address in the branch target address storage register. Dowling defines a branch condition as a condition that indicates whether or not a branch is early-resolvable (*See, Dowling, col. 14, lines 2-4*).

In contrast, as discussed above, amended independent Claim 1 requires that the branch address is an address wherein "a branch to the branch target address occurs when the fetch address is the branch address after a x-th instruction from the branch setting instruction" Applicant respectfully submits that, a branch condition does not teach or suggest "a branch address" as required by amended independent Claim 1.

Accordingly, applicant respectfully submits Dowling fails to disclose, teach or suggest "the branch information setting circuit stores the branch address in a branch address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded," as required by amended independent Claim 1.

The Office Action also states that Dowling at col. 13, lines 2-14, discloses that branch target address comparisons are made to determine whether to output information from saved data, and that this reads on, "the fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result, " as required by amended independent Claim 1 (*See, Office Action. p. 4, line 18-p.5, line 2*).

However, applicant respectfully submits that Dowling at column 13, lines 2-9, discloses that a state machine accepts the early branch indication strobe on the line and at substantially the same time receives at least a part of the branch instruction address on the line. This address information is compared against a set of resident branch cache tags. If the detected branch address matches a tag, then a branch cache hit is said to occur, and control is passed over a from the idle state to a cache hit state; when the branch instruction address does not match a branch cache tag, control is passed over a transition to a state. Applicant respectfully submits that Dowling discloses comparing the branch address, which is a branch instruction address, with branch cache tags.

In contrast, amended independent Claim 1 requires comparing, "one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result." Applicant respectfully submits that comparing a branch instruction address does not teach or suggest comparing with a value stored in the branch address register (i.e., a branch address).

Accordingly, applicant respectfully submits that Dowling fails to disclose, teach or suggest comparing "a value stored in the branch address storage register," as required by amended independent Claim 1 (*See, Office Action, p. 4, line 18-p.5, line* 2).

Since the cited Dowling fails to disclose, teach or suggest the above features recited in amended independent Claim 1, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, amended independent Claim 1 believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that amended independent Claim 2 is allowable for at least the same reasons as discussed above with reference to amended independent Claim 1.

Additionally with regard to amended independent Claim 2, the Office Action states that Dowling at col. 16, lines 25-30 discloses a non-delayed branch instruction is the offset branch address instruction and that this reads on, "wherein the fetch address operation circuit includes a circuit which compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch address storage register or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch address storage register," as required by amended independent Claim 2 (*See, Office Action, p. 5, lines 7 to 15*).

However, applicant respectfully submits that Dowling at col. 16, lines 25 – 30 discloses comparing a non-delayed conditional branch instruction address with branch cache tags. If there is a match, then the branch cache data associated with the matched tag is accessed. Applicant respectfully submits that comparing a non-delayed conditional branch instruction address does not teach or suggest comparing a value stored in the branch address register (i.e., a branch address).

Accordingly, applicant respectfully submits that Dowling fails to disclose, teach or suggest comparing "one of a previous fetch address and an expected next

fetch address with a value stored in the branch address storage register," as required by amended independent Claim 2.

Since the cited Dowling fails to disclose, teach or suggest the above features recited in amended independent Claim 2, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

The remaining Claims 3-18 depend either directly or indirectly from amended independent Claims 1-2 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the remaining Claims 2-18 are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4721 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: July 9, 2007

By: _____
Aniket A. Patel
Registration No. 55,525

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601